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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/602,997	Applicant(s) CHENG, YI	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-116* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9, 11-15, 21-27, 33, 35-39, 45, 48, 52, 53, 57, 60, 64-65, 69, 76-77, 81, 84-85, 91-93, 96-97, 103-105, 108-109, 115-116* is/are rejected.

7)☒ Claim(s) *See Continuation Sheet* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/2003,6/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 47 are objected to because of the following informalities: in claim 1, the recitation of "capable of" in line 12 is not a positive recitation. It is suggested to delete "capable of". In claim 47, the recitation of "460" is suggested to change to --46--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 53 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 53, the recitation of "second programmable control signals" in line 3 is indefinite because it is inconsistent with the limitation set forth in claim 45. Claim 45 calls for first programmable circuit responses to a first programmable control signal. Applicant is required to particularly point out the first programmable control signal, second programmable control signals.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited prior art figure 2. Applicant's cited prior art figure 2 shows a comparator comprising a first input transistor (N4), a first input (In2), first reference voltage (Vss), a current source (S4), a resistor (R2), a second input transistor (In1), a second input (In1), a current source (S3), an output (output) capable of setting toward the first reference voltage when a firs signal at the first input exceeds the hysteresis offset or a second reference voltage when the first signal at the first input does not exceed the hysteresis offset as called for in claim 1.

Regarding claim 2, the hysteresis offset is controllable by varying the value of the resistor R2.

Regarding claim 3, the amount of current generated by the current source S4 is controllable, thereby affecting the hysteresis offset.

3. Claims 1-3, 9, 12-15, 21, 24-27, 33 and 36- 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Bridgewater, Jr. (USP 6,307,401). Figure 8 of Bridgewater, Jr. shows a comparator comprising a first input transistor (414), a first input (82), first reference voltage (Vcc), a current source (440), a resistor (RB), a second input transistor (412), a second input (84), a current source (440), an output (110) capable of setting toward the first reference voltage when a firs signal at the first input exceeds the hysteresis offset or a second reference voltage when the first signal at the first input does not exceed the hysteresis offset as called for in claim 1.

Regarding claim 2, the hysteresis offset is controllable by varying the value of the resistor RB.

Regarding claim 3, the amount of current generated by the current source 440 is controllable by sizing the transistor 440 differently, thereby affecting the hysteresis offset.

Regarding claims 9, 21 and 33, figure 9 of Bridgewater, Jr. shows a comparator comprising a first programmable circuit (510) operable to selectively provide a hysteresis offset in response to a first programmable control signal (output of the control logic 512), a comparator circuit (502), responsive to the first programmable circuit, to receive a first and a second signal (82, 84) and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to results of comparison.

Regarding claims 12, 24 and 36, the first and second signals are mixed.

Regarding claims 13, 25 and 37, the first programmable circuit (510 of figure 9 of Bridgewater, Jr.) includes a programmable impedance elements (516) for selectively setting the hysteresis offset in response to a first programmable circuit control signal (572).

Regarding claims 14-15, 26-27 and 38-39, programmable current source (518) for setting minimal voltage for input signals in response to the first programmable circuit control signal (572).

4. Claim 33 is rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. (USP 6,384,637). Figure 7 of Nguyen et al. shows a device comprising a first programmable circuit (635, 640) operable to selectively provide a hysteresis offset in response to a first programmable control signal (F1, F2), and a comparator circuit (620, 625), responsive to the first programmable circuit, to receive a first and a second signal (Vm, Vref) and compare the first signal and the

second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to result of comparison as called for in claim 33.

5. Claims 45, 48, 52, 53, 57, 60, 64-65, 69, 72 and 76-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrett, Jr. et al. (USP 6,094,075). Figure 7B of Garrett, Jr. shows a programmable comparator comprising a first programmable circuit (switches M1 coupled to capacitors) operable to selectively provide a hysteresis delay in response to a first programmable control signal (signal controls switches M1), a comparator circuit (N5, N6, P9, P10, N71), responsive to first programmable circuit, to receive a first and a second input signals (per-minus, per-plus) in response to the hysteresis delay and provide a digital output signal (Q) in response to result of the comparison between the first and second input signals as called for in claims 45, 48, 52, 57, 60, 64-65, 69, 72 and 76-77.

Regarding claim 53, insofar as understood, the recited "second programmable control signals" is being interpreted as first control signals and is anticipated by control signals control the switches M1.

6. Claims 81, 85, 91, 92, 93, 87, 103, 104, 105, 109, 115 and 116 are rejected under 35 U.S.C. 102(b) as being anticipated by Wohlfarth et al. (USP 5,999,044). Figure 3 of Wohlfarth shows a device comprising a first programmable circuit (current source receives signal Vlow, switch receives signal RANGE, Q7-Q9) operable to selectively providing an output loading on an output circuit (Q1-Q4, R7-R10) in response to a first programmable control signal (Vlow, RANGE) and comparator circuit (12 in figure 20) in communication with the first programmable

circuit to compare a first input signal (INPUT+)a second input signal (INPUT-) and provide a digital output signal in response to result of comparison and the output loading on the output circuit as called for in claims 81, 85, 91, 93, 97, 103, 105, 109 and 115.

Regarding claims 92, 104 and 116 a plurality of current sources Q7-Q10 are selectable in response to the switch receive control signal RANGE.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Fischer et al. (USP 6,459,306). Figure 4B of Fischer et al. shows a comparator comprising a first input transistor (M4), a first input (VPI), first reference voltage (VDD), a current source (M8), a resistor (R2), a second input transistor (M3), a second input (VNI), a current source (M8), an output capable of setting toward the first reference voltage when a first signal at the first input exceeds the hysteresis offset or a second reference voltage when the first signal at the first input does not exceed the hysteresis offset as called for in claim 1.

Regarding claim 2, the hysteresis offset is controllable by varying the value of the resistor R2.

Regarding claim 3, the amount of current generated by the current source is controllable by the size of the transistor M8, thereby affecting the hysteresis offset.

Regarding claim 4, a third transistor (M7) is in communication with the first transistor (M4).

Regarding claim 5, the third electrical path (Mp12, M7) comprises a current source (MP12).

Regarding claim 6, the output of the comparator is the junction of MP12 and M7.

8. Claims 81, 85, 91, 93, 97, 103, 105, 109 and 115 are rejected under 35 U.S.C. 102(e) as being anticipated by Lau et al. (USP 6,462,588). Figure 4 of Lan et al. shows a device comprising a first programmable circuit (186, 188, 190, 192) operable to selectively providing an output loading on an output circuit (182, 184) in response to a first programmable control signal (n01, n02, p01, p01) and comparator circuit (194, 196, 198) in communication with the first programmable circuit to compare a first input signal (vref) and a second input signal (vmid) and provide a digital output signal in response to result of comparison and the output loading on the output circuit as called for in claims 81, 85, 91, 93, 97, 103, 105, 109 and 115.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bridgewater, Jr. (USP 6,307,401). Figure 9 of Bridgewater, Jr. shows a device comprising a first programmable circuit (510) operable to selectively provide a hysteresis offset in response to a first programmable control signal (output of the control logic 512), a comparator circuit (502), responsive to the first programmable circuit, to receive a first and a second signal (82, 84) and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to results of

comparison. Bridgewater, Jr. does not disclose the device is programmable by a user for boundary scan testing as called for in claims 11, 23. It is known in the art comparator circuit are used in boundary scan testing. Bridgewater, Jr.'s comparator is excellent in speed and consume less power. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to program Bridgewater, Jr's comparator for boundary scan testing for the reasons as noted.

10. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (USP 6,384,637).

Figure 7 of Nguyen et al. shows a device comprising a first programmable circuit (635, 640) operable to selectively provide a hysteresis offset in response to a first programmable control signal (F1, F2), and a comparator circuit (620, 625), responsive to the first programmable circuit, to receive a first and a second signal (Vm, Vref) and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to result of comparison. Nguyen et al. does not disclose control signal F1 or F2 is from user as called for in claim 35. However, it is known that the control signals F1 and F2 are inputted from outside of the device. Therefore, it would have been obvious to a person skilled in the art to designate the control signals to be inputted from the user to enhance the flexibility of the device in setting the hysteresis offset. Therefor, outside of non-obvious results, the obviousness of designating the control signal to be inputted by the user is not patentable under 35USC 103(a).

11. Claim 84 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lau et al. (USP 6,462,588). Figure 4 of Lan et al. shows a device comprising a first programmable circuit (186,

188, 190, 192) operable to selectively providing an output loading on an output circuit (182, 184) in response to a first programmable control signal (n01, n02, p01, p01) and comparator circuit (194, 196, 198) in communication with the first programmable circuit to compare a first input signal (vref) and a second input signal (vmid) and provide a digital output signal in response to result of comparison and the output loading on the output circuit. Lau et al. does not disclose control signal (n01, n02, p01, p02) is from user as called for in claim 84. However, it is known that the control signals n01, n02, p01, p02 are inputted from outside of the device. Therefore, it would have been obvious to a person skilled in the art to designate the control signals to be inputted from the user to enhance the flexibility of the device in setting the output loading. Therefor, outside of non-obvious results, the obviousness of designating the control signal to be inputted by the user is not patentable under 35USC 103(a).

12. Claims 84, 96 and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wohlfarth (USP 5,999,044). Figure 3 of Wohlfarth shows a device comprising a first programmable circuit (current source receives signal Vlow, switch receives signal RANGE, Q7-Q9) operable to selectively providing an output loading on an output circuit (Q1-Q4, R7-R10) in response to a first programmable control signal (Vlow, RANGE) and comparator circuit (12 in figure 20) in communication with the first programmable circuit to compare a first input signal (INPUT+)a second input signal (INPUT-) and provide a digital output signal in response to result of comparison and the output loading on the output circuit. Wohlfarth does not disclose first, second and third control signals (RANGE, VLOW, VHIGH) is from user as called for in claim 84. However, it is known that the control signals RANGE, VLOW, VHIGH are inputted from outside of the device. Therefore, it would have been obvious to a person skilled in the art

to designate the control signals to be inputted from the user to enhance the flexibility of the device in setting the output loading. Therefor, outside of non-obvious results, the obviousness of designating the control signal to be inputted by the user is not patentable under 35USC 103(a).

13.

Allowable Subject Matter

14. Claims 7-8, 10, 16-20, 28-32, 34, 40-44, 46-47, 49-51, 54-56, 58-59, 61-63, 66-68, 70-75, 78-80, 82, 86-88, 83, 89-90, 94, 98-100, 95, 101-102, 106, 110-112, 107 and 113-114 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

8/23/2004